



CM214-COMP2008

Data Communications and Networks

Switch Problems & Design

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Objectives



- The Hardware of Packet Switching
 - Why specialised hardware is needed
- (Peterson & Davie 2nd Ed., Section 3.1, 3.2, 3.4)
- (Peterson & Davie 3rd Ed., Section 3.4)



Review



- In the previous units we looked at
 - Ethernet bridges
 - Ethernet switches
 - Routing methods
 - Routing tables and algorithms
- Recall switches (next two slides)



Switch Characteristics



- Ideally, we would like our switch to:
 - Provide multi-way connections
 - To avoid expense & complexity of linking every network with every other by a point-to-point link
 - Be able to connect to other switches
 - For redundancy and scalability
 - Not impose too much of a performance limitation on traffic
 - Keep all the (expensive) p-t-p links busy



Switch Actions



- Receive packets on inbound links
- Send packets on outbound links
- Route packets between links
 - Datagram routing
 - Virtual circuit routing
 - (Source routing – now usually ignored as security risk)



Switch Congestion



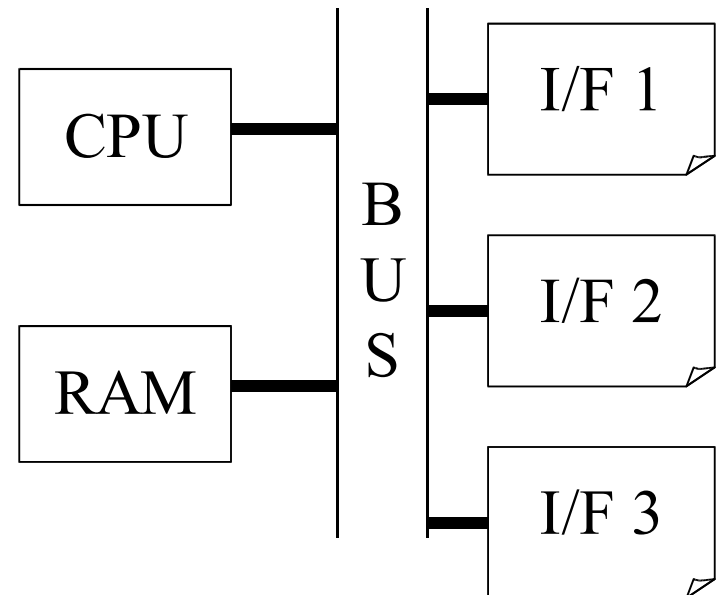
- Switches need to buffer packets
 - Because packets may arrive faster than they can be sent out - Why?
 - May have different speeds on each port
 - > 1 inbound port may have packets for same outbound port
 - Buffers may fill up – Possible solutions
 - Virtual circuits can pre-allocate buffer space
 - Throw packets away
 - Share buffer space between ports



PCs as Switches - 1



- Can we use a PC or workstation as a switch?
- On receipt of packet
 - CPU gets interrupt
 - DMA data into RAM
 - Read & decode header
 - Place in output queue





PCs as Switches - 2



- To send the output packet:
 - output I/F interrupts CPU when ready
 - CPU programs DMA transfer to I/F
 - Packet is sent
- Limitation is either memory or I/O (bus) bandwidth
- Most PCs / workstations designed to support a single I/F
 - Typical bandwidth 50-100Mb/s TOTAL



PCs as Switches - 3



- Recall, optical links run from 50Mb/s to 2.48Gb/s (& ever higher)
- For maximum we want to keep each link full of data
- Therefore, most ports will be operating near capacity
- PC architecture does not support necessary bus bandwidth



Switch Performance



- What are we trying to achieve?
 - Throughput
 - Lots of packets switched per second
 - Scalability
 - Lots of ports (interfaces)
 - Cost
 - Minimise costs of manufacture
 - Minimise costs of operation



Switch Throughput



- Depends on the type of traffic
- E.g. Contention for a single output port will limit performance to the speed of that port
- Size of packets
- Packet arrival times
 - Steady or “bursty”

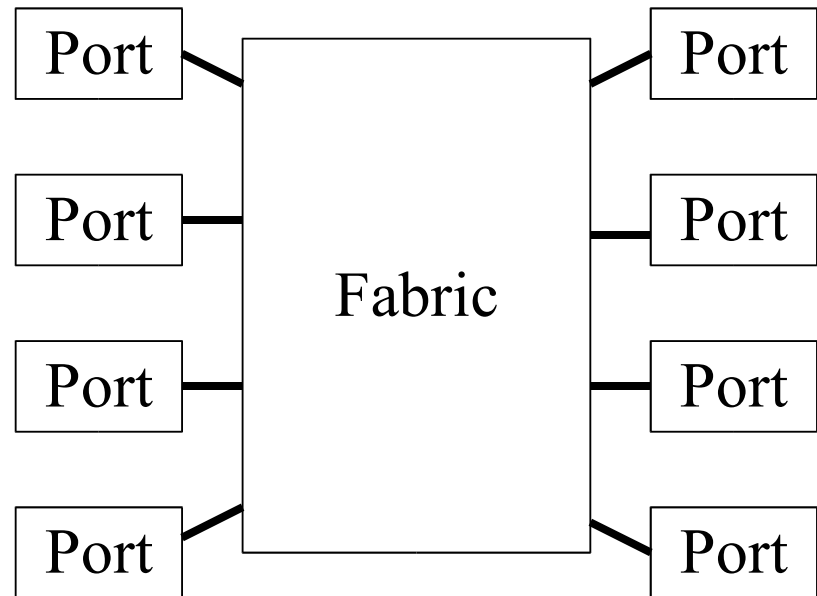


Switch Design



- How is necessary throughput achieved?

- Complicated ports
- Simple (and hence FAST) fabric





Port Implementation



- Usually no input buffering
 - Due to “head of line blocking”
- Must do the mapping to the output port
- Output buffering
- Implements QOS guarantees



Fabrics – Crossbar



- Connect inputs to all outputs
- Ports setup control logic for multiplexors appropriately
- Does not scale well
- Output buffer must deal with contention



Fabrics – Shared Media



- Modified PC architecture, dedicated HW
- Big pool of shared buffers in RAM
- Very wide memory access to give sufficient bandwidth (wide bus)
- Limitation probably speed of control logic



Fabrics – Banyan / Batchers



- Self routing network within fabric
- Makes small, simple (**fast!**) decisions
 - Net result is correct output port
- Banyan network routes packet through set of nodes without collisions provided packets sorted in numerical order
- Batchers is hardware to sort packets in numerical order of output port



Banyan Limitations



- Does not solve problem of contention
 - Output ports must still buffer
- Solution
 - Use multiple banyans
 - Don't drop packets on contention
 - Delay them and re-inject into banyan network



Summary



- Switches are specialised hardware devices
- General purpose computers (PCs, workstations) do not make good switches